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# Scalable fabrication of $PtSe_2$ metal-semiconductor lateral junctions via local layer engineering

Two-dimensional (2D) transition metal dichalcogenides (TMDs), such as $MoS_2$ and $WSe_2$, have been considered as promising new channel materials in future electronic devices for further scaling down the transistor size and thickness in integrated circuits. However, the performance of field-effect transistors (FETs) based on TMD materials is still considerably limited by the low carrier mobility and the high metal contact resistance. Recently, focused attentions have been redirected to noble metal dichalcogenides (such as $PtSe_2$ and $PdS_2$), which also belong to the TMD family, but exhibit a very strong layer-dependent electronic properties. Of particular interest is 2D PtSe2, whose properties can vary from a semiconductor with a sizable bandgap in the monolayer limit to a semimetal as the thickness is increased to few layers, due to the strong interlayer coupling [1]. The layer tunable bandgap in $PtSe_2$ is very appealing, since the manipulation between a semiconducting phase and a metallic phase can be achieved by layer engineering. Electronic devices based on exfoliated few-layer $PtSe_2$ have been demonstrated [2] and showed metallic and semiconducting behaviors for thick and thin layers, respectively. However, devices based on mechanical exfoliation is not scalable, and unlikely to achieve local layer engineering. Wafer-scale $PtSe_2$ films have also been obtained by direct selenization of Pt films [3]. However, precise control of layer thickness is difficult for the selenized films, particularly for only 1-2 monolayer thick. In this work, we report a facile method to synthesize large-area $PtSe_2$ films with controlled thickness by chemical vapor deposition (CVD). Electrical characterizations confirmed that thick $PtSe_2$ films are metallic and exhibit a low contact resistance, while thin PtSe2 films (1-2 ML) are semiconductor and show a large current modulation via electrostatic gating. We also demonstrate that contact regions of thin $PtSe_2$ films can be converted into metallic phase by local patterning regrowth, representing a scalable fabrication process to form $PtSe_2$ metal-semiconductor lateral junctions via local layer engineering.

Large-area $PtSe_2$ films (up to $2\times2$ $cm^2$, see Fig. 1A) with controlled thickness (0.8-20 nm) were grown at low temperatures (350-450 °C) on sapphire substrates by CVD using Se and $PtCl_2$ as precursors. The thickness have been identified by atomic force microscopy, as shown in Fig. 1B. Raman measurements can also be used to identify the layer thickness. Two characteristic peaks at ~180 and ~208.5 $cm^{-1}$, which correspond to the $E_g$ and $A_{1g}$ Raman modes of $PtSe_2$, respectively, show a red shift and an increasing intensity ratio $A_{1g}/E_g$ as the thickness was increased from 0.8 to 16 nm, as shown in Fig. 1C. Figure 1D shows the transmission electron microscopy image, where the 1T hexagonal structure with a lattice constant of 0.37 nm can be identified. We have fabricated the FET devices based on 0.8-nm $PtSe_2$ films gated by using ion gel ([EMIM]-[TFSI]). Figure 2A shows the room-temperature transfer curve ($I_d$-$V_g$) of a 0.8-nm-thick $PtSe_2$ FET using ionic gating. A current on-off ratio higher than $10^2$ is observed and a field-effect mobility of ~3 $cm^2V^{-1}s^{-1}$ is deduced. For the thicker $PtSe_2$ film using Ni as the contact metal [4], a low contact resistance of 772 Ω·μm and a sheet resistance of 921 Ω/□ are achieved, which is shown in Fig. 2B. The feature of low temperature growth further enable us to proceed patterning growth of $PtSe_2$ using a shadow mask (e.g. a patterned SiO2 film) as shown in Fig. 2C. The success of patterning growth also demonstrate the feasibility of fabricating $PtSe_2$ metal-semiconductor lateral junction via local layer engineering. As illustrated in Fig. 2D, a monolayer $PtSe_2$ with a

sizable bandgap can act as the channel material, while the contact areas can be converted into metallic phase by patterning regrowth, where the thick $PtSe_2$ with low contact resistances can further boost the device performance for practical applications.

## Figures

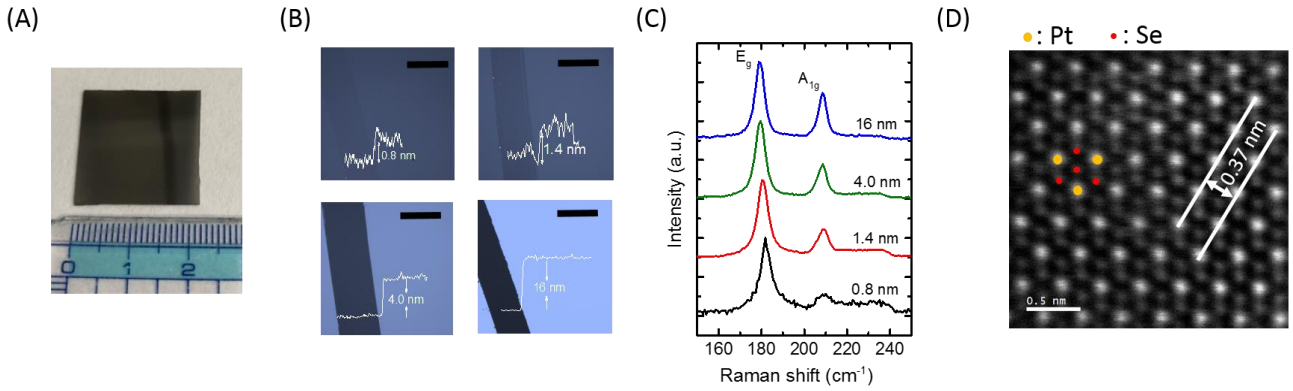


**Figure 1:** (A) An optical image for a CVD grown $PtSe_2$ film on a sapphire substrate. (B) Optical microscope images and AFM line scans for $PtSe_2$ film with different thicknesses. The scale bar is 5 μm. (C) Raman spectra $PtSe_2$ films with thicknesses of 0.8, 1.4, 4.0 and 16 nm. (D) A TEM image of the CVD-grown $PtSe_2$ film.

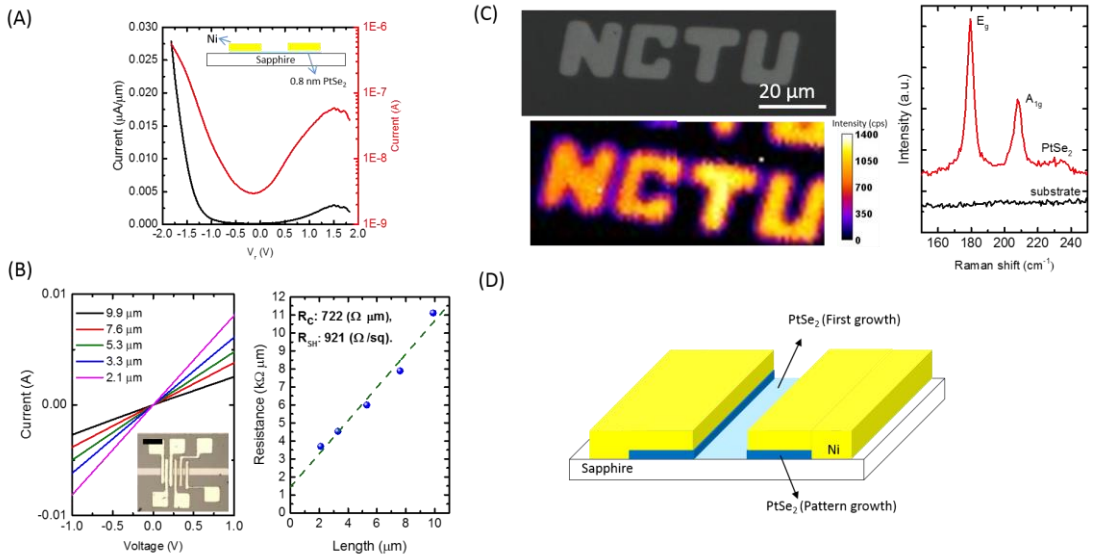


**Figure 2:** (A) The transfer curve ($I_{ds}$- $V_r$) of a 0.8-nm-thick $PtSe_2$ FET device. (B) The contact resistance determined by transfer-length method for a 10-nm-thick $PtSe_2$ with the Ni as the contact metal. (C) Optical image and Raman mapping of patterned-grown $PtSe_2$. (D) A schematics for the device structure fabricated by local layer engineering.

## References


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