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Large area graphene synthesis on CMOS compatible materials

Abstract

Graphene and graphene-based devices have demonstrated great potential to extend the functionality of a large variety of microelectronic applications [1, 2]. However, the successful integration of these novel devices into "CMOS environments" is strongly dependent on several key challenges, like handling, cleaning, contacting, patterning as well as non-destructive depositions of dielectric layers on graphene. Among these challenges, the availability of wafer-scale high quality graphene on CMOS compatible materials (dielectrics or semiconductors) is of highest importance. Therefore, in this paper, we examine the potential of 200 mm, in-house grown epitaxial Ge(100)/Si(100) and structured Ni/SiO_2 substrates for the development of Si-CMOS compatible graphene synthesis methods. It should be also stressed that the experiments in this work were carried out in a standard BiCMOS pilot-line, making this study unique, as its results might directly pave the way to further graphene integration and graphene-based device prototyping in mainstream Si technologies. As a first investigated substrate, germanium (Ge) has shown the potential as an alternative substrate for graphene growth [3-5], due to its catalytic activity, extremely low solubility of carbon and availability of large area Ge on Si [6]. In this work, CVD experiments have been performed at a deposition temperature of 885 °C using CH_4 as carbon source. The Raman results are shown in Fig. 1, where good quality graphene was detected over the entire Ge(100)/Si(100) substrate. A detailed surface morphology study was carried out by SEM and STM. Graphene-induced Ge faceting is clearly recognizable as a result of adsorbed hydrogen on the surface as proved by DFT calculations. The extracted electrical values for the transferred layers (from the Ge/Si substrates onto 100 nm SiO_2/Si substrates) were Rs ~1500 ±100 Ω/sq and μ ~400 ±20 $cm^2/V{\cdot}s$. Recently, it has been demonstrated that electronic as well as mechanical properties of the graphene are influenced by the orientation of the germanium crystal [7]. As an optimization approach towards improved rotational alignment of graphene on Ge(110), we will also present the results from the preparation of Ge(110)/Si(110) wafers and graphene growth on them.

As a second approach, we show the developments of a transfer-free, Ni-mediated graphene synthesis method on insulating SiO_2 substrates. The potential of Ni as a mediator for graphene synthesis has already been investigated by several groups so far, where graphene films were grown via chemical vapor and solid deposition methods at elevated temperatures (~1000 °C) [8-10]. In these cases, graphene growth occurred on top of Ni, underneath Ni and between Ni dots. Although these approaches are very promising, the control of the quality, number of layers and defects in graphene is a real challenge. In this work, the CVD experiments were performed in the temperature range of 800 – 1000 °C, using C_2H_4 gas as the source of carbon and Ar as a carrier gas. As shown in Fig. 3, graphene could be also successfully grown on insulating SiO_2 layers, if Ni is employed as a catalyst. The full development details and complementary electrical characterizations of both approaches (graphene on Ge and Ni) will be presented in this work.

References

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Figures

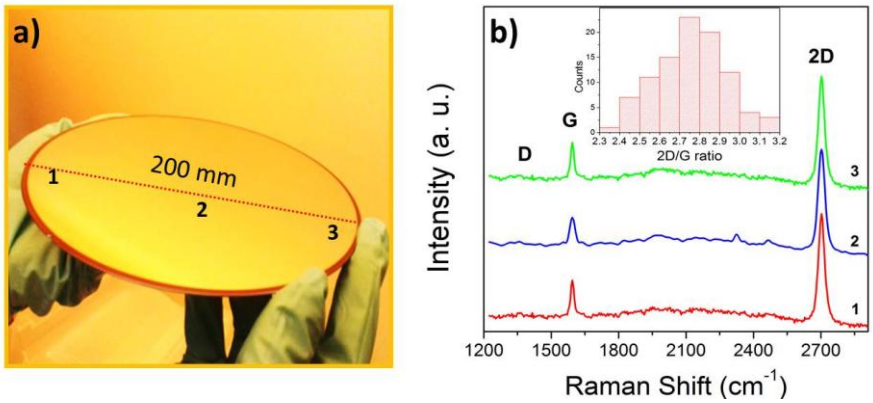

Figure 1: Fig. 1 (a) Graphene grown on 200 mm Ge/Si wafer and (b) Raman spectra from the indicated measurement locations. The histogram of the 2D/G ratio over the entire wafer (~100 measured points) is depicted in the inset of Fig.1 b).

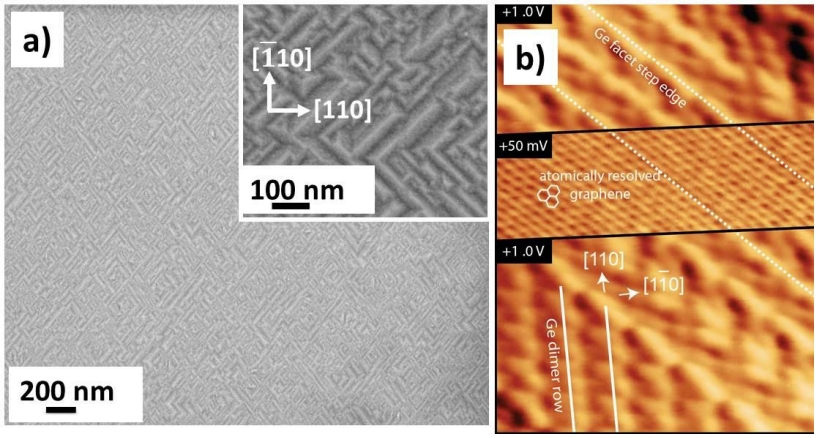

Figure 2: (a) SEM and (b) STM images of the graphene on Ge(001).

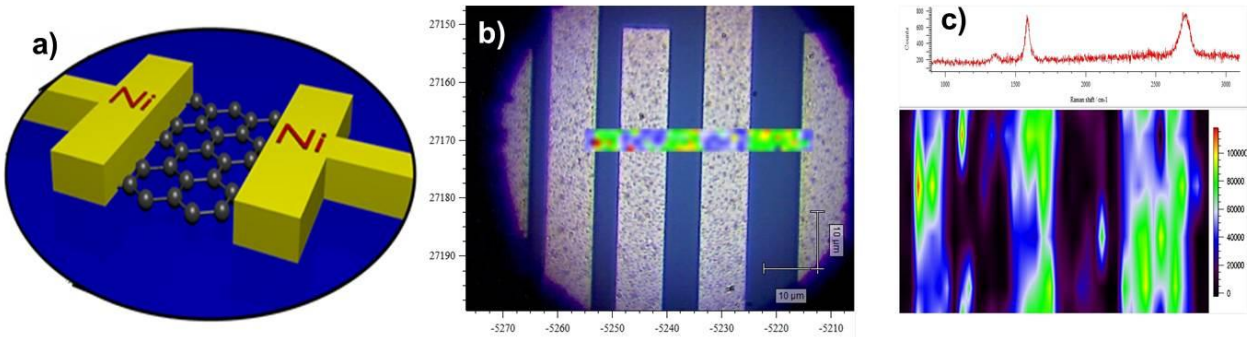

Figure 3: (a) Graphical representation of the Ni-assisted Graphene synthesis, (b) optical image of graphene, overlapped with Raman 2D intensities and (c) Raman mapping of the 2D intensity of the graphene.